CLAIM LISTING

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously presented) An integrated circuit comprising:

a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of a first external filter, and a second pair of bonding pads for conducting a differential input signal thereon and-configured to be coupled to an output of said first external filter; and

an integrated circuit package encapsulating said semiconductor substrate and having first and second terminal pairs corresponding and coupled to said first and second pairs of bonding pads, respectively,

wherein said first and second terminal pairs are separated by a first predetermined distance sufficient to maintain an input-to-output isolation therebetween of at least a first predetermined amount, and wherein said first predetermined amount corresponds to a first electrical characteristic of said first external filter.

2. (Previously presented) The integrated circuit of claim 1, wherein said first predetermined amount corresponds to an attenuation in a stopband of said first external filter.

3. (Previously presented) The integrated circuit of claim 1, wherein said first and second terminal pairs are located along a first side of said integrated circuit package and separated by a first plurality of intervening terminals.

4. (Previously presented) The integrated circuit of claim 3, wherein said first plurality of intervening terminals comprises twelve terminals.

5. (Previously presented) The integrated circuit of claim 3, wherein said first plurality of intervening terminals comprises at least one power supply terminal.

6. (Previously presented) The integrated circuit of claim 3, wherein first and second terminals of said first terminal pair are adjacent to one another, and first and second terminals of said second terminal pair are adjacent to one another.

7. (Previously presented) The integrated circuit of claim 6, wherein said first and second terminal pairs are located at opposite ends of said first side of said integrated circuit package.

8. (Previously presented) The integrated circuit of claim 1, wherein:

said semiconductor substrate further has a third pair of bonding pads conducting a differential output signal thereon and configured to be coupled to an input of a second external filter, and a fourth pair of bonding pads conducting a differential input signal thereon and configured to be coupled to an output of said second external filter;

said integrated circuit package further has third and fourth terminal pairs corresponding and coupled to said third and fourth pairs of bonding pads, respectively; and

said third and fourth terminal pairs are separated by a second predetermined distance sufficient to maintain an input-to-output isolation therebetween of at least a second predetermined amount, wherein said second predetermined amount corresponds to a second electrical characteristic of said second external filter.

9. (Previously presented) The integrated circuit of claim 8, wherein said first and second predetermined amounts correspond to differences between an attenuation in stopbands of said first and second external filters respectively.

10. (Previously presented) The integrated circuit of claim 8, wherein said first and second terminal pairs are located along a first side of said integrated circuit package and separated by a first plurality of intervening terminals and said third and fourth terminal pairs are located along a second side of said integrated circuit package and separated by a second plurality of intervening terminals.

11. (Previously presented) The integrated circuit of claim 10, wherein said first and second pluralities of intervening terminals each comprises twelve terminals.

12. (Previously presented) The integrated circuit of claim 10, wherein said first and second pluralities of intervening terminals each comprises at least one power supply terminal.

13. (Previously presented) The integrated circuit of claim 10, wherein first and second terminals of each of said first, second, third, and fourth terminal pairs are adjacent to one another.

14. (Previously presented) The integrated circuit of claim 10, wherein said first and second terminal pairs are located at opposite ends of said first side of said integrated circuit package and said third and fourth terminal pairs are located at opposite ends of said second side of said integrated circuit package.

15. (Previously presented) An integrated circuit comprising:

a semiconductor substrate having first, second, third, and fourth quadrants having respective first, second, third, and fourth bonding pads located therein, said semiconductor substrate including a first circuit-configured to be coupled to a first external filter coupled to said first circuit through said first and second bonding pads, and a second circuit-configured to be coupled to a second external filter coupled to said second circuit through said third and fourth bonding pads; and

an integrated circuit package encapsulating said semiconductor substrate and having first, second, third, and fourth terminals corresponding and coupled to said first, second, third, and fourth bonding pads, respectively, wherein said first terminal and said second terminal are separated by a first distance sufficient to maintain a first input-to-output isolation therebetween that is based on a first electrical characteristic of said first external filter, and wherein said third terminal and said fourth terminal are separated by a second distance sufficient to maintain a second input-to-output isolation therebetween that is based on a second electrical characteristic of said second external filter.

16. (Previously presented) The integrated circuit of claim 15, wherein said first and second circuits comprise portions of radio frequency (RF) receivers.

17. (Previously presented) The integrated circuit of claim 16, wherein said first circuit comprises a portion of a satellite receiver and said second circuit comprises a portion of a terrestrial receiver.

18. (Previously presented) The integrated circuit of claim 16, wherein said first and second circuits have substantially the same layout.

19. (Previously presented) The integrated circuit of claim 15, wherein said first and second circuits are configured to be coupled to first and second external surface acoustic wave (SAW) filters, respectively.

20. (Previously presented) The integrated circuit of claim 15, wherein said semiconductor substrate further comprises fifth, sixth, seventh, and eighth bonding pads respectively located in said first, second, third, and fourth quadrants and forming complementary signal pairs with signals conducted on said first, second, third, and fourth bonding pads, respectively.

21. (Previously presented) An integrated circuit comprising:

a semiconductor substrate having a first pair of bonding pads for conducting a differential output signal thereon and configured to be coupled to an input of an external filter, and a second pair of bonding pads for conducting a differential input signal thereon and configured to be coupled to an output of said external filter; and

an integrated circuit package encapsulating said semiconductor substrate and having at least first and second sides, and comprising a first pair of terminals located at a first end of said first side and coupled to said first pair of bonding pads, and a second pair of terminals located at a second end of said first side opposite said first end and coupled to said second pair of bonding pads, wherein said first pair of terminals and said second pair of terminals are separated by a distance sufficient to maintain an input-to-output isolation therebetween that is based on an electrical characteristic of said external filter.

22. (Previously presented) The integrated circuit of claim 21, wherein said integrated circuit package comprises four sides.

23. (Previously presented) The integrated circuit of claim 22, wherein said integrated circuit package further comprises a thin quad flat package (TQFP).

24. (Previously presented) The integrated circuit of claim 23, wherein said integrated circuit package further comprises a 64-lead TQFP.

25. (Previously presented) The integrated circuit of claim 21, wherein said semiconductor substrate further has a third pair of bonding pads conducting a second differential output signal thereon and-configured to be coupled to an input of a second external filter, and a fourth pair of bonding pads conducting a second differential input signal thereon and-configured to be coupled to an output of said second external filter, and said integrated circuit package further has a third pair of terminals located on a first end of said second side and coupled to said third pair of bonding pads, and a fourth pair of terminals located on a second end of said second side opposite said first end and coupled to said fourth pair of bonding pads.

26. (Previously presented) An integrated circuit comprising:

adjacent first and second terminals at a first end of a first side of the integrated circuit configured to be coupled to a differential input of a first external filter;

adjacent third and fourth terminals at a second end of said first side of the integrated circuit-configured to be coupled to a differential output of said first external filter, wherein said adjacent first and second terminals and said adjacent third and fourth terminals are separated by a first distance sufficient to maintain an input-to-output isolation therebetween that is based on a first electrical characteristic of said first external filter;

adjacent fifth and sixth terminals at a first end of a second side of the integrated circuit configured to be coupled to a differential input of a second external filter; and

adjacent seventh and eighth terminals at a second end of said second side of the integrated circuit-configured to be coupled to a differential output of said second external filter, wherein said adjacent fifth and sixth terminals and said adjacent seventh and eighth terminals are separated by a second distance sufficient to maintain an input-to-output isolation therebetween that is based on a second electrical characteristic of said second external filter.

27. (Previously presented) The integrated circuit of claim 26, wherein the integrated circuit comprises a quad flat package.

28. (Previously presented) The integrated circuit of claim 27, wherein said quad flat package comprises sixty four terminals having corresponding pin numbers assigned consecutively around a periphery of said quad flat package starting from a pin one corner, and wherein said first and second terminals correspond to pins one and two, said third and fourth terminals correspond to pins fifteen and sixteen, said fifth and sixth terminals correspond to pins forty seven and forty eight, and said seventh and eighth terminals correspond to pins thirty three and thirty four.

29. (Previously presented) The integrated circuit of claim 26, wherein each of said first and second external filters comprises a surface acoustic wave (SAW) filter.